TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Abstract of the Disclosure

A CMOS-compatible FET has a reduced electron affinity polycrystalline or microcrystalline SiC gate that is electrically isolated (floating) or interconnected. The SiC material composition is selected to establish the barrier energy between the SiC gate and a gate insulator. In a memory application, such as a flash EEPROM, the SiC composition is selected to establish a lower barrier energy to reduce write and erase voltages and times or accommodate the particular data charge retention time needed for the particular application. In a light detector or imaging application, the SiC composition is selected to provide sensitivity to the desired wavelength of light. Unlike conventional photodetectors, light is absorbed in the floating gate, thereby ejecting previously stored electrons therefrom. Also unlike conventional photodetectors, the light detector according to the present invention is actually more sensitive to lower energy photons as the semiconductor bandgap is increased.